| |
|---|
| 1.INST_NAME indicate the IO_MUX REGISTER defined in eagle_soc.h，for example MTDI_U refers to PERIPHS_IO_MUX_MTDI_U |
| 2.NET NAME accords with the pin name in schematic |
| 3.FUNCTION says the multifunction of each pin pad |
| func number 1-5 in this table correspond to FUNCTION 0-4 in SDK |
| e.g.：set MTDI to GPIO12 |
| [1]#define FUNC_GPIO12  3 //defined in eagle_soc.h |
| [2]PIN_FUNC_SELECT(PERIPHS_IO_MUX_MTDI_U,FUNC_GPIO12); |

| | F | G | K | L | M | N | O | P | Q | R | S | T | U |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | PDUW08D | MTDI_U | MTDI | I | I2SI_DATA | I/O/T | HSPIQ M | I/O/T | GPIO12 | I/O/T | U0DTR | O | oe=0, wp |
| 3 | PDUW08D | MTCK_U | MTCK | I | I2SI_BCK | I/O/T | HSPID M | I/O/T | GPIO13 | I/O/T | U0CTS | I | oe=0, wp |
| 4 | PDUW08D | MTMS_U | MTMS | I | I2SI_WS | I/O/T | HSPICLK | I/O/T | GPIO14 | I/O/T | U0DSR | I | oe=0, wp |
| 5 | PDUW08D | MTDO_U | MTDO | O/T | I2SO_BCK | I/O/T | HSPICS | I/O/T | GPIO15 | I/O/T | U0RTS | O | oe=0, wp |
| 6 | PDUW08D | U0RXD_U | U0RXD | I | I2SO_DATA | I/O/T | | O | GPIO3 | I/O/T | CLK_XT | O | oe=0, wp |
| 7 | PDUW08D | U0TXD_U | U0TXD | O | SPICS1 | I/O/T | | O | GPIO1 | I/O/T | CLK_R | O | oe=0, wp |
| 8 | PDUW08D | SD_CLK_ | SD_CLK | I | SPICLK | I/O/T | | O | GPIO6 | I/O/T | U1CTS | I | oe=0 |
| 9 | PDUW08D | SD_DATA | SD_DAT/ | I/O/T | SPIQ | I/O/T | | O | GPIO7 | I/O/T | U1TXD | O | oe=0 |
| 10 | PDUW08D | SD_DATA | SD_DAT/ | I/O/T | SPID | I/O/T | | O | GPIO8 | I/O/T | U1RXD | I | oe=0 |
| 11 | PDUW08D | SD_DATA | SD_DAT/ | I/O/T | SPIHD | I/O/T | | O | GPIO9 | I/O/T | HSPIHI | I/O/T | oe=0 |
| 12 | PDUW08D | SD_DATA | SD_DAT/ | I/O/T | SPIWP | I/O/T | | O | GPIO10 | I/O/T | HSPIW | I/O/T | oe=0 |
| 13 | PDUW08D | SD_CMD | SD_CMD | I/O/T | SPICS0 | I/O/T | | O | GPIO11 | I/O/T | U1RTS | O | oe=0 |
| 14 | PDUW08D | GPIO0_U | GPIO0 | I/O/T | SPICS2 | I/O/T | | O | | I/O/T | CLK_O | O | oe=0, wp |
| 15 | PDUW08D | GPIO2_U | GPIO2 | I/O/T | I2SO_WS | I/O/T | U1TXD | O | | I/O/T | U0TXD | O | oe=0, wp |
| 16 | PDUW08D | GPIO4_U | GPIO4 | I/O/T | CLK_XTAL | O | | | | | | | oe=0 |
| 17 | PDUW08D | GPIO5_U | GPIO5 | I/O/T | CLK_RTC | O | | | | | | | oe=0 |

| Num | Pin | Address | Bit[8] Function Select[2] | Bit[7] Pullup | Bit[6] Rsvd | |
|---|---|---|---|---|---|---|
| 1 | MTDI_U | 0x60000804 | | 0 | 1 | 0 |
| 2 | MTCK_U | 0x60000808 | | 0 | 1 | 0 |
| 3 | MTMS_U | 0x6000080C | | 0 | 1 | 0 |
| 4 | MTDO_U | 0x60000810 | | 0 | 1 | 0 |
| 5 | U0RXD_U | 0x60000814 | | 0 | 1 | 0 |
| 6 | U0TXD_U | 0x60000818 | | 0 | 1 | 0 |
| 7 | SD_CLK_U | 0x6000081C | | 0 | 0 | 0 |
| 8 | SD_DATA0_U | 0x60000820 | | 0 | 0 | 0 |
| 9 | SD_DATA1_U | 0x60000824 | | 0 | 0 | 0 |
| 10 | SD_DATA2_U | 0x60000828 | | 0 | 0 | 0 |
| 11 | SD_DATA3_U | 0x6000082C | | 0 | 0 | 0 |
| 12 | SD_CMD_U | 0x60000830 | | 0 | 0 | 0 |
| 13 | GPIO0_U | 0x60000834 | | 0 | 1 | 0 |
| 14 | GPIO2_U | 0x60000838 | | 0 | 1 | 0 |
| 15 | GPIO4_U | 0x6000083C | | 1 | 0 | 0 |
| 16 | GPIO5_U | 0x60000840 | | 1 | 0 | 0 |

| | | | Bit[6] Function Select[2] | |
|---|---|---|---|---|
| 17 | XPD_DCDC | 0x600007A0 | | 0 |

| Bit[5:4] Function Select[1:0] | Bit[3] Sleep Pullup | Bit[2] Rsvd | Bit[1] Sleep Sel | Bit[0] Sleep OE | GPIO pin |
|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 GPIO12 |
| | 0 | 0 | 0 | 0 | 0 GPIO13 |
| | 0 | 0 | 0 | 0 | 0 GPIO14 |
| | 0 | 0 | 0 | 0 | 0 GPIO15 |
| | 0 | 0 | 0 | 0 | 0 GPIO3 |
| | 0 | 0 | 0 | 0 | 0 GPIO1 |
| | 0 | 0 | 0 | 0 | 0 GPIO6 |
| | 0 | 0 | 0 | 0 | 0 GPIO7 |
| | 0 | 0 | 0 | 0 | 0 GPIO8 |
| | 0 | 0 | 0 | 0 | 0 GPIO9 |
| | 0 | 0 | 0 | 0 | 0 GPIO10 |
| | 0 | 0 | 0 | 0 | 0 GPIO11 |
| | 0 | 0 | 0 | 0 | 0 GPIO0 |
| | 0 | 0 | 0 | 0 | 0 GPIO2 |
| | 0 | 0 | 0 | 0 | 0 GPIO4 |
| | 0 | 0 | 0 | 0 | 0 GPIO5 |

| Bit[5] Sleep Pulldown | Bit[4] Rsvd | Bit[3] Pulldown | Bit[2] Rsvd | Bit[1:0] Function Select[1:0] | |
|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 RTC_GPIO0 |

after reset, the default is function5 to export the clock

after reset, the default is function5 to export U0TXD

| | |
|---|---|
| U0TXD | Strapping to chip_test_mode |

| | |
|---|---|
| MTDO | Strapping to STRAPPING_GPIO2 for SW boot_sel [2] |
| GPIO0 | Strapping to STRAPPING_GPIO1 for SW boot_sel [1] |
| GPIO2 | Strapping to STRAPPING_GPIO0 for SW boot_sel [0] |

| | |
|---|---|
| SD_DATA3 | Strapping to STRAPPING_GPIO[15] for SW sdio_boot_sel [2] |
| SD_DATA2 | Strapping to STRAPPING_GPIO[14] for SW sdio_boot_sel [1] |
| SD_DATA0 | Strapping to STRAPPING_GPIO[13] for SW sdio_boot_sel [0] |

| Boot_sel | SD_sel != 3'b010 |
|---|---|
| 7 | SDIO HighSpeed V2 IO |
| 6 | SDIO LowSpeed V1 IO |
| 5 | SDIO HighSpeed V1 IO |
| 4 | SDIO LowSpeed V2 IO |
| 3 | FLASH BOOT |
| 2 | Jump Boot |
| 1 | UART Boot |
| 0 | Remapping |

| | |
|---|---|
| GPIO0 | after reset, the default is function5 to export the clock |
| GPIO2 | U0TXD signal can be output through GPIO2 pad besides U0TXD pad |

1: normal mode; 0: chip_test_mode

| SD_sel == 3'b010 |
| --- |
| Uart1 Booting |
| Uart1 Booting |
| Uart1 Booting |
| Uart1 Booting |